KAKATIYA INSTITUTE OF TECHNOLOGY & SCIENCE :: WARANGAL-15

(An Autonomous Institute under Kakatiya University, Warangal)

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

One Week Faculty Development Programme (FDP)

on

"VLSI Design using Cadence Tools"

May 16, 2022 - May 20, 2022

SCHEDULE

DAY - 1 (16-05-2022) MONDAY	**SESSION – 1 (10 AM – 1 PM)** ➢ Introduction to Full Custom IC Design Flow ➢ Cadence Solutions for Custom IC Design ➢ Schematic Capture using Virtuoso Schematic Editor ➢ Symbol Creation ➢ Test-bench Creation using Virtuoso Schematic Editor ➢ Functional Simulation using Spectre	**LUNCH BREAK**	**SESSION – 2 (2 PM – 5 PM)** ➢ Layout Design using Virtuoso Layout Editor ➢ Physical Verification which includes DRC & LVS ➢ Parasitic Extraction using Quantus ➢ Post Layout Simulation ➢ Generation of GDSII
DAY - 2 (17-05-2022) TUESDAY	**SESSION – 3 (10 AM – 1 PM)** ➢ Introduction to Semi-Custom IC Design Flow ➢ Cadence Solutions for Semi-Custom IC Design ➢ Functional Simulation using Incisive ➢ RTL Synthesis using Genus Synthesis Solution		**SESSION – 4 (2 PM – 5 PM)** ➢ Physical Implementation using Innovus that includes *Floor Planning *Power Planning *Placement *CTS *Routing ➢ Timing Analysis ➢ Power Analysis ➢ Parasitic Extraction ➢ Generation of GDSII
DAY - 3 (18-05-2022) WEDNESDAY	**SESSION – 5 (10 AM – 1 PM)** ➢ Introduction to STA ➢ Timing Analysis using Innovus ➢ STA Basic flow using TEMPUS tool		**SESSION – 6 (2 PM – 4 PM)** ➢ Introduction to Low power ➢ Power Analysis using VOLTUS ➢ Basic flow using VOLTUS tool
DAY - 4 (19-05-2022) THURSDAY	**SESSION – 7 (11 AM – 1 PM)** ➢ Introduction to Functional Verification ➢ Functional Verification using Conformal LEC ➢ Basic flow of logic equivalence checking		**SESSION – 8 (2 PM – 4 PM)** ➢ Introduction to Design for Test (DFT) ➢ DFT using Modus tool ➢ Basic flow of DFT/ATPG/BIST
DAY - 5 (20-05-2022) FRIDAY	**SESSION – 9 (10 AM – 1 PM)** ➢ Assessment Test ➢ Valedictory		----

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